AMENDMENTS TO THE CLAIMS

Claims 1-18: (Canceled)

19. (Currently Amended) An apparatus comprising:

a substrate comprising a first lattice structure;

a strain-inducing layer disposed on the substrate having a second lattice structure different than the first lattice structure; and

a strained layer disposed on the strain-inducing layer,

wherein the strain-inducing layer and the strained layer are disposed in a channel region for a transistor device and the second lattice structure is defined by a lateral contraction or expansion of the strain-inducing layer,

wherein when the strain-inducing layer comprises silicon germanium[;],

germanium comprises between approximately 20 and 25 percent of the silicon germanium.

20. (Previously Presented) The apparatus of Claim 19, further comprising:

a gate electrode disposed on the strained layer;

a first spacer disposed adjacent to a first side of the gate electrode; and

a second spacer disposed adjacent to a second side of the gate electrode,

wherein the strain-inducing layer and the strained layer comprises lateral edges defined by an edge of the first spacer and an edge of the second spacer.

21. (Canceled)

22. (Canceled)

23. (Original) The apparatus of Claim 19, wherein the apparatus comprises:

an n-type metal oxide semiconductor.

24. (Original) The apparatus of Claim 23, wherein the strain-inducing layer comprises:
silicon germanium.

25. (Original) The apparatus of Claim 24, wherein germanium comprises between approximately 20 and 25 percent of the silicon germanium.

26. (Original) The apparatus of Claim 24, wherein the silicon germanium layer has a thickness of between approximately 400 and 500 Å.

27. (Original) The apparatus of Claim 26, wherein the strained layer comprises silicon and has a thickness of between approximately 100 and 200 Å.

28. (Original) The apparatus of Claim 19, wherein the apparatus comprises:
a p-type metal oxide semiconductor.

29. (Original) The apparatus of Claim 28, wherein the strain-inducing layer comprises:
silicon carbide.

30. (Original) The apparatus of Claim 29, wherein carbon comprises between approximately 1 and 2 percent of the silicon carbide.

31. (Currently Amended) A system comprising:
an integrated circuit package comprising
a substrate comprising a first lattice structure,
a strain-inducing layer disposed on the substrate, the strain-inducing layer comprising a second lattice structure different than the first lattice structure, and
a strained layer disposed on the strain-inducing layer,
wherein the strain-inducing layer and the strained layer are disposed in a channel region for a transistor device and the second lattice structure is defined by a lateral contraction or expansion of the strain-inducing layer,
wherein when the strain-inducing layer comprises silicon germanium[;],

germanium comprises between approximately 20 and 25 percent of the silicon germanium.

32. (Original) The system of Claim 31, wherein the system comprises:
an n-type metal oxide semiconductor.

33. (Original) The system of Claim 32, wherein the strain-inducing layer comprises:
silicon germanium.

34. (Original) The system of Claim 33, wherein germanium comprises between approximately 20 and 25 percent of the silicon germanium.

35. (Original) The system of Claim 31, wherein the system comprises:
a p-type metal oxide semiconductor.

36. (Original) The system of Claim 35, wherein the strain-inducing layer comprises:
silicon carbide.

37. (Original) The system of Claim 36, wherein carbon comprises between approximately 1 and 2 percent of the silicon carbide.